IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Currently Amended) A method allowing a choice of Least Frequently Used (LFU) or Most Frequently Used (MFU) cache line replacement, the method comprising the steps of:

determining new state information for at least two given cache lines of a plurality of cache lines in a cache, the new state information based at least in part on prior state information for the at least two given cache lines; and

when an access miss occurs in one of the at least two given lines:

selecting either LFU or MFU replacement criteria, wherein said selection is based on a selection signal; and

replacing one of the at least two given cache lines based on the new state information and the selected replacement criteria.

2. (Original) The method of claim 1, wherein the step of selecting further comprises the step of selecting either LFU or MFU replacement criteria based on selection information.

3. (Original) The method of claim 1, wherein:

the state information comprises a plurality of line use counters, each line use counter corresponding to one of the plurality of cache lines; and

the step of determining new state information further comprises the step of incrementing a given line use counter when a cache line corresponding to the given line use counter is referenced.

4. (Original) The method of claim 3, where the reference to the cache line corresponding to the given line use counter is a hit reference.

5. (Original) The method of claim 3, wherein:

the plurality of cache lines are assigned to a plurality of congruence classes, each congruence class assigned to at least two of the plurality of cache lines, whereby at least two of the line use counters corresponds to a congruence class;

the state information further comprises a plurality of congruence class use counters; and

the step of determining new state information further comprises the step of incrementing a given one of the plurality of congruence class use counters when a congruence class corresponding to the given congruence class use counter is referenced, wherein each of the plurality of congruence class use counters corresponds to one of the congruence classes.

6. (Original) The method of claim 5, wherein the reference to the congruence class corresponding to the given congruence class use counter is a hit reference.

7. (Original) The method of claim 5, wherein:

the plurality of line use counters are also assigned to the plurality of congruence classes, one line use counter per cache line assigned to a congruence class; and

the step of determining new state information further comprises the step of, when one or more of the line use counters corresponding to a given congruence class exceeds a maximum line use counter limit, dividing all of the line use counters corresponding to the given congruence class by an integer.

8. (Original) The method of claim 7, where the integer is a power of 2.

9. (Original) The method of claim 5, wherein:

a given congruence class corresponds to a given congruence class use counter; and

the step of determining new state information further comprises the steps of, when the given congruence class use counter exceeds a maximum congruence class use counter limit:

dividing all of the line use counters corresponding to the given congruence class by an integer; and

resetting the given congruence class use counter.

10. (Original) The method of claim 9, where the integer is a power of 2.

11. (Original) The method of claim 5, wherein the cache is an n-way set associative cache, whereby there are n cache lines per congruence class.

12. (Original) The method of claim 3, wherein the step of determining new state information further comprises the steps of:

inverting a predetermined number of line use counters;

selecting, based on the step of selecting either LFU or MFU replacement criteria, either values of the predetermined number of line use counters or the inverted versions of the predetermined number of line use counters, wherein the values of the predetermined number of line use counters are selected for an LFU calculation and the inverted versions of the predetermined number of line use counters are selected for an MFU calculation; and

determining which of the values of the predetermined number of line use counters or the inverted versions of the predetermined number of line use counters is smallest in value.

13. (Currently Amended) A cache allowing a choice of Least Frequently Used (LFU) or Most Frequently Used (MFU) cache line replacement, the cache comprising:

a plurality of cache lines;

state information for at least two given cache lines of the plurality of cache

lines;

LFU/MFU circuitry adapted:

to determine new state information for at least two given cache lines of a plurality of cache lines in a cache, the new state information based at least in part on prior state information for the at least two given cache lines;

when a cache miss occurs in one of the at least two given lines:

to select either LFU or MFU replacement criteria, wherein said selection is based on a selection signal; and

to determine which one of the at least two given cache lines should be replaced based on the new state information and the selected replacement criteria; and

replacement circuitry coupled to the LFU/MFU circuitry and to the plurality of cache lines, the replacement circuitry adapted to replace the selected given cache line.

14. (Original) The cache of claim 13, wherein the LFU/MFU circuitry further comprises selection circuitry, and wherein the selection circuitry is adapted to select either the LFU or MFU replacement criteria.

15. (Previously Presented) The cache of claim 13, wherein:

the state information comprises a plurality of line use counters, each line use counter corresponding to one of the cache lines; and

the LFU/MFU circuitry is further adapted to increment a given line use counter when a cache line corresponding to the given line use counter is referenced.

16. (Original) The cache of claim 15, where the reference to the cache line corresponding to the given line use counter is a hit reference.

17. (Original) The cache of claim 15, wherein the plurality of cache lines are assigned to a plurality of congruence classes, each congruence class assigned to at

least two of the plurality of cache lines, whereby at least two of the line use counters corresponds to a congruence class, the state information further comprising a plurality of congruence class use counters, each of the congruence class use counters corresponding to one of the congruence classes, and wherein the LFU/MFU circuitry is further adapted to increment a given congruence class use counter when a congruence class corresponding to the given congruence class use counter is referenced.

18. (Original) The cache of claim 17, wherein the reference to the congruence class corresponding to the given congruence class use counter is a hit reference.

19. (Original) The cache of claim 17, wherein the plurality of line use counters are also assigned to the plurality of congruence classes, one line use counter per cache line assigned to a congruence class, and wherein the LFU/MFU circuitry is further adapted, when one or more of the line use counters corresponding to a given congruence class exceeds a maximum line use counter limit, to divide all of the line use counters corresponding to the given congruence class by an integer.

20. (Original) The cache of claim 19, where the integer is a power of 2.

21. (Original) The cache of claim 17, wherein a given congruence class corresponds to a given congruence class use counter, and wherein the LFU/MFU circuitry is further adapted, when the given congruence class use counter exceeds a maximum congruence class use counter limit, to divide all of the line use counters corresponding to the given congruence class by an integer and to reset the given congruence class use counter.

22. (Original) The cache of claim 21, where the integer is a power of 2.

23. (Original) The cache of claim 17, wherein the cache is an n-way set associative cache, whereby there are n cache lines per congruence class.

24. (Original) The cache of claim 15, wherein the LFU/MFU circuitry further comprises:

a multiplexer (MUX) coupled to a predetermined number of line use counters and to inverted versions of the predetermined number of line use counters, the MUX adapted to select, as a predetermined number of outputs, either values of the predetermined number of line use counters or the inverted versions of the predetermined number of line use counters;

an LFU detector coupled to the predetermined number of outputs of the MUX and adapted to determine which of the predetermined number of outputs is smallest in value, the LFU detector producing one or more LFU outputs, wherein the one or more LFU outputs are coupled to the replacement circuitry; and

selection circuitry coupled to the MUX and adapted to cause the MUX to select either the values of the predetermined number of line use counters or the inverted versions of the predetermined number of line use counters.

25. (Previously Presented) A cache for replacing Most Frequently Used (MFU) cache lines, the cache comprising:

a plurality of cache lines;

state information for at least two given cache lines of the plurality of cache lines, wherein said state information includes at least one relative MFU count;

MFU circuitry adapted:

to produce new state information for the at least two given cache lines in response to an access to one of the at least two given cache lines and to maintain said at least one relative MFU count to indicate a frequency of use of at least one of said given cache lines relative to one or more of said given cache lines; and

when a cache miss occurs in one of the at least two given cache lines to determine, based on the new state information, which of the at least two

given cache lines is the most frequently used cache line; and

replacement circuitry coupled to the MFU circuitry and to the plurality of cache lines, the replacement circuitry adapted to replace the given cache line determined as the most frequently used.

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26. (Previously Presented) The cache of claim 25 wherein said MFU circuitry is further adapted to adjust said at least one relative MFU count when said at least one relative MFU count exceeds a maximum threshold.